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(54) **Gated transmission circuit (on-chip)**

(57) A gated binary signal transmission circuit in a field effect semiconductor chip comprises a single signal-pass transistor (20A, B) connected between a bit signal input line (28A, B) and a bit signal output line (12A, B). The control electrode (22A, B) of the transistor (20A, B) receives energisation pulses from a control circuit (32, 34) at prescribed intervals and conduction between energisation pulses will persist, though with some decay, due to inherent capacitance and the control electrode being left "floating" between energisations. The transmission circuit is used to control a programmable logic or bistable circuit.

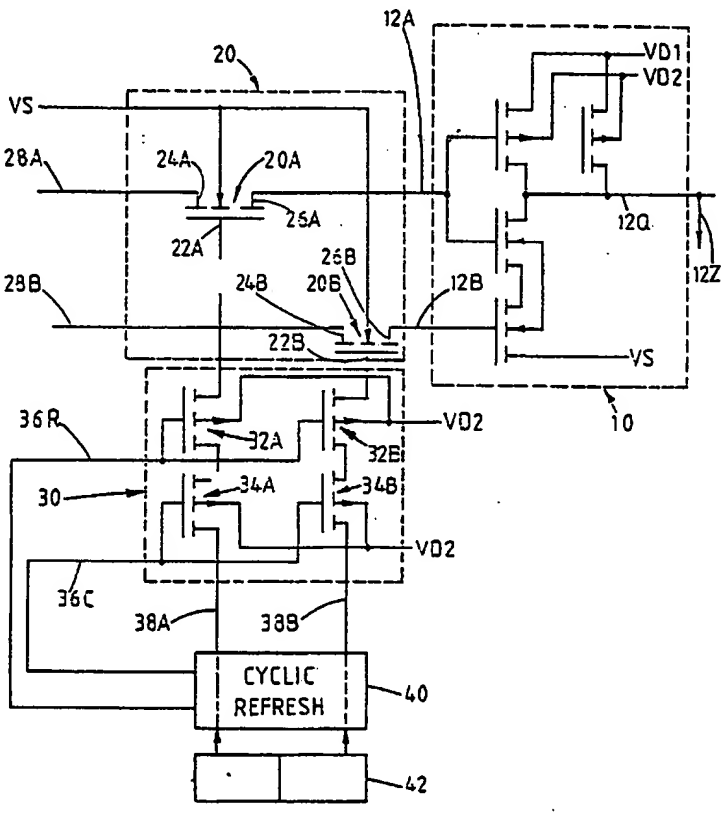

FIG.1.

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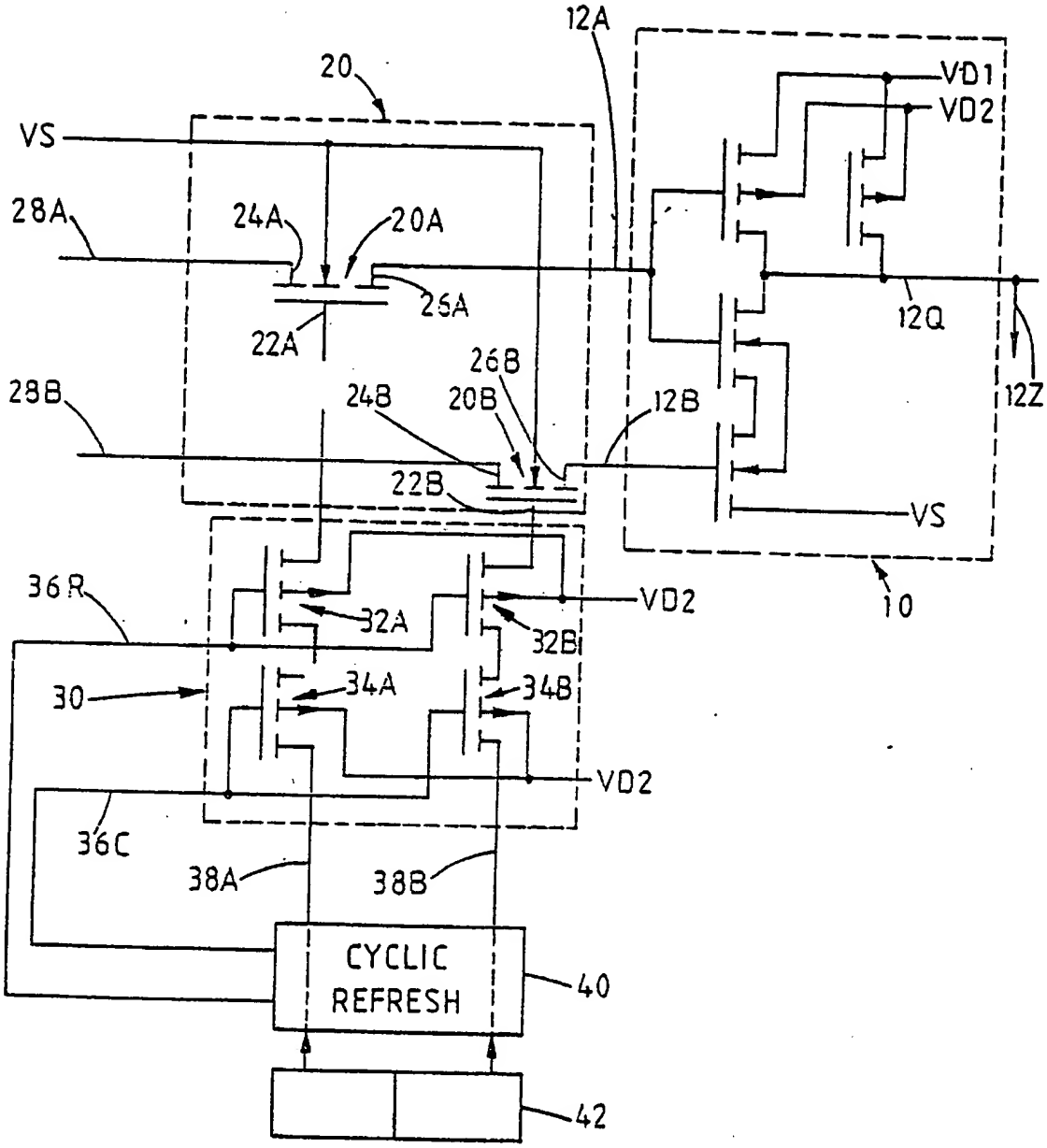
12A
20
VD1
VD2
VS
28A
24A
20A
26A
22A
12Q
12Z
26B
28B
24B
20B
12B
22B
VS
10
36R
VD2
32A
32B
30
34A
34B
VD2
36C
38A
38B
CYCLIC
REFRESH
40
42

FIG.1.

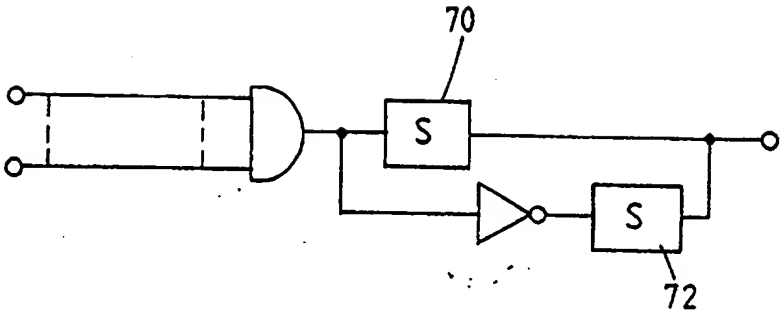

FIG.2A.

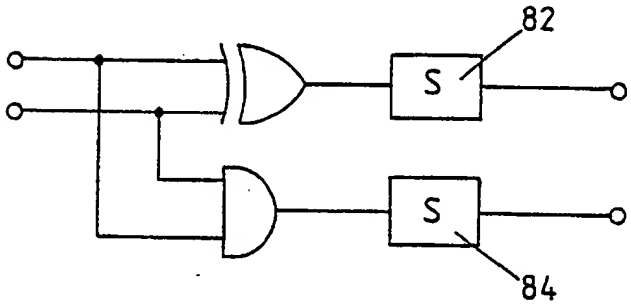

FIG.2B.

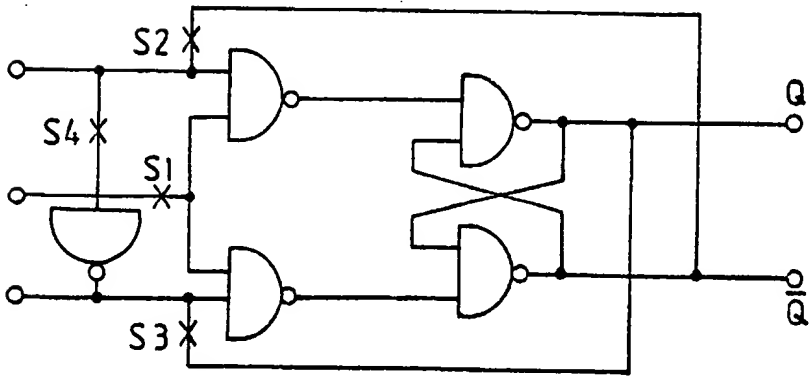

FIG.2C.

SPECIFICATION

Gated transmission circuit (on-chip)

Description

This invention relates to electronic circuitry of semiconductor integrated circuits and has particular reference to providing a gated digital signal transmission circuit that is efficiently implemented in semiconductor field effect integrated circuits.

It is inherent in field effect semiconductor technology that capacitance is associated with all circuit elements, as formed, i.e. not only with formation of passive circuit elements such as specifically-formed capacitors, but also with active circuit elements, such as p-channel and n-channel transistors. Much attention has been directed on the one hand to reducing such capacitance for switching type transistors in order to improve speed of operation, and on the other hand to devising transistor element structures that trap electrons and then hold and exhibit a capacitive charge virtually permanently.

So-called MOS has become a popular technology for digital semiconductor field effect integrated circuits (chips) used in computers and allied data processing industries. Developments of the original metal-oxide-semiconductor substrate construction include substituting enhanced conduction semiconductors, e.g. polysilicon, for metal, and incorporation of other layers such as nitride (MNOS). Examples of the wide application of MOS include read-only memories (ROMs), whether of programmable type (ROMs) or re-programmable type (EPROMs), and writable memories of dynamic type (DRAMs).

Fast switching is important for DRAMs where it is customary for each bit storage site to include a switching transistor of lowest achievable inherent capacitance and an associated with a specific capacitor formation. The capacitor formation stores one binary value (normally '1) when the capacitor element is charged, and otherwise represents the other binary value. Charging or not is controlled by the state of the switching transistor at writing to the memory. Reading is by sensing the state of charge as a voltage and using high impedance sensing circuitry. The capacitor charge will decay but is periodically restored in so-called refresh cycles each normally involving a read operation to sense the capacitor charge state followed by a re-write operation to those sites storing binary '1' values.

Charge trapping is important for EPROMs where charge trapping transistors are each usually associated with load circuit formations. Appropriate trapped charge applied at higher than normal operating logic levels can prevent such a transistor from switching. Non-destructive reading can be by attempted switching and sensing whether or not there is a voltage drop across the associated load. Trapped charges of so-called floating gate or nitride oxide sandwich transistors can be discharged by signals of higher voltage levels than logic levels used for normal chip-operation, or by irradiation, whereupon they are ready for rewriting of the EPROM. Writing, erasing and rewriting is usually carried out by special-purpose equipments, known as EPROM writers.

Where it is required to pass a binary value representative signal in field effect chips, such as CMOS, it is customary to use a so-called transmission gate. Such a CMOS transmission gate typically comprises at least four transistors for signal passage namely a p-channel transistor and a n-channel transistor in parallel each to pass a different one of the two binary value signals and two other transistors acting as an inverter. There may be as many as four more transistors forming a latch to set the state of the transmission gate on a stored-state basis of operation (which would be required together with further transistors for selection purposes in relation to later-discussed programmable logic array chips).

It will be appreciated that reading from DRAM chips involves effectively sensing a voltage condition for each bit site which voltage condition is dependent on stored capacitive charge. It will be further appreciated that such sensing is quite different from requirements of a transmission gate in that the latter must effectively pass signals from its input to its output, i.e. reproduce recognisable and operative equivalent signals, normally logic "high" and logic "low".

There is a need for much simpler transmission gate circuitry. Thus, without it, attempts to improve the capability of programmable logic array chips (PLAs), appear to involve increasing the complexity of logic cells, especially if ready reprogrammability is to be obtained in actual operation on a reconfigurable basis.

The long-established PLA chips devoted much of their active areas to formation of a matrix of all possible connections of gate inputs and outputs with generally irreversible interconnection selection at crossing points and with the actual gate circuits generally restricted to edges of those areas. It is only possible significantly to improve the gate capacity of PLAs by reducing the area devoted to interconnection relative to that devoted to logic circuitry, and, particularly, by distributing the logic circuitry cells more evenly over the active chip areas. We have, ourselves, proposed a new and advantageous configurable logic chips for PLAs with a substantially uniform distribution of logic circuits, preferably simple conventional logic gates each having a single logic function. However, to achieve in-situ reconfigurability there is a problem if conventional transmission gates or multiplexers are used for interconnection purposes as they each need too much chip area to be able to service individual inputs and outputs of a reasonable number of simple logic gate circuits. It is believed to be particularly advantageous to be able to use simple logic gates, for example two-input NAND gates. Accepting such limitations leads to providing large and functionally configurable logic circuitry cells on the chip, but in relatively small numbers, and thus with less flexibility and/or familiarity for circuit designers used to designing for ULAs.

It is an object of this invention to provide relatively simple signal-transmission circuitry for field effect semiconductor chips.

According to this invention a gated binary signal transmission circuit in a field effect semiconductor chip comprises a single signal-pass transistor con-

nected between a bit signal input to one of its electrodes and a bit signal output from another of its electrodes and having a control electrode (by energisation of which conduction is normally established between the first and second electrodes) connected for temporary energisations by switching circuitry operative only at prescribed intervals, the single signal-pass transistor being operative to pass signals between said energisations of its control electrode. Those energisations render the single signal-pass transistor conductive, i.e. enabled for conduction, and that conduction is caused to persist, though with some decay, hence periodic refreshing at said prescribed intervals. Inherent capacitance of the single signal-pass transistor inevitably results in accumulation of charge during each said energisation applied to its control electrode. The switching circuitry operates, not to apply discharge voltage between such energisations at said prescribed intervals, but rather to leave the control electrode "floating" between refreshes by said energisations. Such single signal-pass transistors are, of course, capable of continuous signal passage despite only intermittent energisation of their control electrodes.

Embodiments of this invention are particularly useful in providing inputs to or outputs from logic gate circuitry on the same chip, particularly to determining whether or not such input or output is to be capable of receiving or providing a bit signal. Application to programmable logic arrays will be evident, i.e. selecting whether or not a possible connection path to a logic gate input or from its output is or is not conducting. For conduction, periodic energisation of the control electrode forces saturation of the single signal-pass transistor, and intervals between such energisations are kept short enough not to lose its 'on' state, i.e. to recur before inherently arising capacitve charge drains away to an extent preventing any significant conduction. Another switchable transistor is suitable for controlling application of said energisation, and it is feasible to have a further switchable transistor in series therewith, or replace those two switching transistors by a dual-gate MOSFET, in order to provide for coincident current selection for the purposes of enabling energisations of the associated single signal-pass transistor. Such provision is particularly useful in arranging that enablement takes place synchronously with reading out a relevant bit location of a ROM (one bit location per signal-pass transistor) and actual energisation depends on the bit value stored at that location.

The single signal-pass transistor hereof represents a dramatic simplification compared with conventional transmission gates. Also, compared with action of a DRAM bit storage site, there is effectively storage and switching in the same transistor. Further compared with a DRAM, there is no provision for a read operation prior to each refresh as the required conduction state will be known from externally available signals or memory contents representing a prescribed configuration.

Actual capacitance at a field effect transistor of a chip depends upon geometries and materials of the MOS transistor formation, and it is further proposed herein that signal-pass transistors be formed such as to enhance capacitance, at least relative to other (switching) transistor formations of the chip (which can follow the main line of development towards reducing capacitance). Then, intervals between refreshes may be longer and/or voltage fidelity of output-to-input bit signals improved. It is, however, emphasised that viable implementation of this invention results using standard chip fabrication techniques for CMOS at 3-micron feature size and with said specific intervals of about 1 millisecond.

It will be appreciated that single signal pass transistor circuitry hereof may not operate with the usual voltage fidelity associated with prior transmission gates, typically giving logic "high" at 5 volts and logic "low" at 0 volts, due to transistor threshold level effects (referred to in the art as VT). That can be met by using suitably different operating voltage, i.e. to give normal logic level output signals (see below), or by accepting a lower speed of operation of an associated logic circuit if such logic circuit, say a simple logic gate, is so operable below normally specified voltage (which it often is).

Using n-channel for the single-pass transistor, threshold level effects, including so-called "body-effect", result in degradation of a high level logic signal. Allowance needs to be made for at least one transistor threshold level, so that substantially more than the currently commonplace +5 volts (for logic "high") will be required. However, using a p-channel signal- pass transistor, (for which "body effect" contribution to VT is less), degradation will effectively be at logic 'low' level, i.e. will not need more than normal logic "high" level (5 volts) to turn fully off and, further, will not need more than - 5 volts to turn the p-channel 'on' even via two switching transistors.

It may be seen as advantageous to operate between +5 volts and −5 volts rather than between a voltage substantially greater than +5 volts and zero. There is basic compatibility with the normal logic "high" level, and requirement for power supply also with the equivalent negative level is quite trivial technically and economically, and there would, in any event, be only low current consumption at −5 volts compared with the rest of the chip.

It is apparent that minimum feature sizes and widths associated with MOS transistor implementation will decrease as integrated circuit technology continues to develop, say from 3-micron to 1.5-micron even 1 - micron, and consequently allow inherently faster response. That would result in acceptable speed for lower logic voltages. Then, it is feasible to use n-channel single signal-pass transistors, as will be specifically described.

Specific implementation of this invention will now be described by way of example with reference to the accompanying drawings, in which Figure 1 shows a circuit diagram for a logic gate site with its gate inputs having selectable connections using this invention; and Figures 2A-2C show application to configurable logic circuits.

In the drawings, referring first to Figure 1, the circuitry shown is readily implemented in a CMOS chip. Section 10 shows four transistors in a generally conventional circuit configuration operative as a two-input NAND gate having inputs 12A and 12B and

output 12Q, but with supply voltages VD1, VD2 and substrate voltage VS applied as discussed further below. Section 20 shows n-channel single signal-pass transistors of this invention at 20A and 20B to pass signals for inputs 12A and 12B, respectively, of the gate 10. Section 30 shows switching transistors for energising control electrodes (gates) 22A and 22B of the single signal-pass transistors, and shown in pairs 32A and 34A, 32B and 34B for coincident current selection of the single signal-pass transistors 20A, 20B via the lines 36R and 36C.

The single signal-pass transistors 20A and 20B have their source and drain electrodes 24A, 26A and 24B, 26B, respectively, connected in series between the gate inputs 12A and 12B and signal lines 28A and 28B, respectively. The single signal-pass transistors 20A and 20B determine whether or not signals on the lines 28A, 28B, respectively, are passed in a recognisable and operative manner to the gate inputs 12A, 12B. If either of the transistors 20A, 20B is enabled for conduction it will pass bit signals, otherwise not.

Either of the single signal pass transistors 20A and 20B can be saturated and thus rendered capable of conducting if the corresponding switching transistors 32A, 34A and 32B, 34B are themselves enabled for conduction by signals on lines 36R and 36C, and a suitable energising signal is available on the corresponding one of energisation lines 38A and 38B. Presence or asbence of a suitable voltage level on energising lines 38A, 38B determines whether or not the corresponding single signal pass transistor 20A, 20B is turned 'on'.

For the n-channel signal-pass transistors shown in the drawing, and for logic gate operation below the customary +5 volts (for logic "high",) but at the customary 0 volts (for logic "low"), VD1 can be +3 volts with VD2 at +5 volts and VS at zero volts. For p-channel signal-pass transistors (not shown), the corresponding voltages would be +5 volts for VD1 and VD2, zero volts at VS for the logic gate, but with −5 volts at VS for the signal-pass transistors.

The energising lines 38A, 38B are shown coming from refresh circuitry 40 serving to apply signals to the energising lines 38 at prescribed intervals, say in accordance with the contents of a latch register 42, which could be an external store location or indeed any source of appropriate binary signals of which one value represents 'on' and the other "off" for the single signal pass transistors 20A, 20B. The refresh circuitry 40 is also shown, for convenience, as supplying enabling selection signals to the lines 36R and 36C.

It will be appreciated that the simplest circuit hereof would be with only a single switching transistor, say 32A, present, and only coincidence of signals on lines 36R and 38A required for turning 'on' the transistor 32A. In fact, the line 38A could then be permanently connected to a suitable voltage level for applying energising signal whenever the switching transistor 32A was turned 'on'. Then, of course, refreshing could be entirely by periodic application of signals on line 36R, which switch the transistor 32A 'on' only if the single signal-pass transistor 20A is to be enabled for passing signals.

Importantly hereto, the dynamic nature of the illustrated transmission gates, each comprised of a single signal-pass transistor 20 and switching circuitry 32 or 32, 34, requires (when conduction is to be enabled) refreshing at intervals such that the single signal-pass transistor remains sufficiently conductive to pass an effective signal to the connected gate input 12. Such passing action thus applies at and during cyclic refreshing. Between refreshes, the line 38 is left "floating".

At first setting up of a conduction state for a single signal-pass transistor 20 hereof, it will switch by saturation of its channel due to switching on transistors 32 and 34 and in the presence of energisation signal on line 38. In the process of doing so, a capacitive charge inevitably builds up due to "holes" (electrons for a p-channel) signal-pass transistor) injected through its control electrode 22 that tend to discharge after transistors 32, 34 switch off in order to go non-conductive. Before that happens the transistor 32 34 will be switched on again and the signal on line 38 re-applied for a short time in order to re-saturate the channel of the single signal- pass transistor (20). Effectively, there are repetitive write cycles to maintain the state of the single signal-pass transistor relative to a reference determined via the energisation line.

Branches 12X and 12Y from the inputs 12A, 12B indicate use of single signal pass transistor circuitry hereof for choosing input lines other than 28A and 28B, respectively, as enabled feeds to the two-input NAND gate 10. Choice of outputs might be similarly provided for from branch 12Z.

One application envisaged is, of course, in relation to improved PLAs, particularly of a type (to which we have other relevant patent applications) where their logic gates are distributed substantially evenly over a chip in a matrix array. Then, each logic gate site could correspond to Figure 1, say with some inputs 10A, 10X directly from prescribed other gates and other such inputs from longer range connection paths (typically row and column following) to which branch outputs 12A, 12X can also be selectably connected.

Self-evidently, there are other applications wherever user- or machine-selection of connections to modify or control a chip's action is desirable. For example, it may be desired to provide complex and configurable logic cells, which clearly offer scope for using embodiments of this invention to set up desired ones of possible connections, for particular logic configurations, say instead of signal-path-switching type circuits for choosing which of possible outputs shall receive an input signal. Very simple examples are shown in Figures 2A, B, C.

In Figure 2A, selection circuitry (described above for 30 or 50) could be used at 70, 72 to allow choice of a true AND function or a NAND function.

In Figure 2B, selection circuitry can be used relative to a half-adder circuit on its outputs (see 82, 84) to give a choice of half-adder if two outputs are to be allowed (both 82 and 84 conducting) or Exclusive-OR (only 82 conducting) or AND (only 84 conducting) functions, at least for single output logic.

In Figure 2C, selection circuitry can be used relative to flip-flop circuitry and selection circuitry this time

shown as crosses and labelled S1 to S4. A basic SR flip-flop obtains if all selection circuits S1 to S4 are off, a clocked SR flip-flop if only S1 is conducting, a D-type when only S1 and S4 are conducting, and a T-type when only S4 is off.

CLAIMS

1. A field effect semiconductor integrated circuit includes at least one gated binary signal transmission circuit formation comprising a single signal-pass transistor connected between a bit signal input to one of its electrodes and a bit signal output from another of its electrodes and switching circuitry to which its conduction control electrode is connected for energisations each only temporarily but following each other at prescribed intervals, the signal-pass transistor being operative to pass signals between successive said energisations relying on conduction persisting due to inherent and undischarged capacitance of the signal-pass transistor.

2. An integrated circuit according to claim 1, wherein the switching circuitry includes a first further field effect transistor connected to be enabled for conduction of signals determining said energisations of said conduction control electrode of the single signal-pass transistor, otherwise to leave the conduction control electrode floating.

3. An integrated circuit according to claim 2, wherein the switching circuitry includes a second further field effect transistor connected with the first further transistor to control enablement of the latter for conduction in accordance with two enabling signals.

4. An integrated circuit according to claim 3, wherein the second further transistor is connected in series with the first further transistor, and to be enabled for said conduction so that the signal-pass transistor is energised for conduction only when both of the further transistors are enabled on a coincident basis and an energisation signal is applied via said further transistors.

5. An integrated circuit according to any one of claims 2 to 4, wherein said further transistor or transistors are of a channel type opposite to that of the signal-pass transistor.

6. An integrated circuit according to any one of claims 2 to 5, further comprising refresh control circuitry operative repetitively at appropriate intervals to supply enabling signals to said switching circuitry.

7. An integrated circuit according to claim 6, further comprising a latch register controlling supply of energisation signals.

8. An integrated circuit, according to any preceding claim, further comprising a logic circuit whose inputs and/or outputs include selectable connection paths each containing a said single signal-pass transistor.

9. An integrated circuit according to any preceding claims, wherein the inherent gate capacitance or the or each signal-pass transistor is enhanced relative to other transistors of the integrated circuit.

10. A field effect semiconductor integrated circuit having at least one signal transmission circuit formation substantially corresponding to the circuit shown in the drawing.

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